AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A liquid crystal display comprising:

a thin film transistor plate further comprising:

a gate line on a first transparent substrate,

a data line arranged to cross the gate line wherein the gate line is insulated from the data line,

a gate electrode protruding from said gate line in an area where said data line crosses said gate line,

a thin film transistor having a source electrode connected to the data line and a drain electrode separated from the source electrode wherein the source and drain electrodes confront each other,

a passivation layer covering the thin film transistor wherein a contact hole exposing a portion of the drain electrode is formed in the passivation layer, and

a pixel electrode formed on the passivation layer and being connected to the drain electrode through the contact hole, wherein the pixel electrode partially overlaps the data line;

a color filter plate including a black matrix, a color filter and a common electrode on a second transparent substrate; and

liquid crystals [[injected]] provided and sealed between the thin film transistor plate and the color filter plate,

wherein the black matrix of the color filter plate asymmetrically overlaps the data line of the thin film transistor plate.

2. (Original) The liquid crystal display according to the claim 1, wherein a location where the black matrix overlaps the data line is selected according to a direction of rubbing an alignment film.

3. (Original) The liquid crystal display according to the claim 1, wherein the passivation layer is an organic passivation layer.

4. (Original) The liquid crystal display according to the claim 3, wherein the organic passivation layer is made of acryl.

5. (Original) The liquid crystal display according to the claim 3, wherein the organic passivation layer is made of BCB.

6. (Currently Amended) A liquid crystal display comprising:

a thin film transistor plate further comprising:

a gate line on a first transparent substrate,

a first data line arranged to cross the gate line wherein the gate line is insulated from the data line,

a gate electrode protruding from said gate line in an area where said data line crosses said gate line,

a thin film transistor having a source electrode connected to the first data line and a drain electrode separated from the source electrode wherein the source and drain electrodes confront each other,

a passivation layer covering the thin film transistor wherein a contact hole exposing a portion of the drain electrode is formed in the passivation layer, and

a pixel electrode formed on the passivation layer and being connected to the drain electrode through the contact hole, wherein the pixel electrode partially overlaps the first data line at a first end of the pixel electrode;

a color filter plate including a black matrix, a color filter and a common electrode on a second transparent substrate; and

liquid crystals [[injected]] provided and sealed between the thin film transistor plate and the color filter plate,

wherein the pixel electrode asymmetrically overlaps a second data line at a second end of the pixel electrode opposite the first end.

7. (Original) The liquid crystal display according to claim 6, wherein an overlap width between the first data line and the pixel electrode is between 2μm and 4μm, and wherein an overlap width between the pixel electrode and the second data line is less than 2μm.

8. (Currently Amended) The liquid crystal display according to claim 6, wherein [[the]] an overlap width between the pixel electrode and the first data line is selected according to a direction of rubbing an alignment film.

9. (Original) The liquid crystal display according to claim 6, wherein the passivation layer is an organic passivation layer.

10. (Currently Amended) A liquid crystal display comprising:

a thin film transistor plate further comprising:

a gate line on a first transparent substrate,

a data line arranged to cross the gate line wherein the gate line is insulated from the data line,

a gate electrode protruding from said gate line in an area where said data line crosses said gate line,

a thin film transistor having a source electrode connected to the data line and a drain electrode separated from the source electrode wherein the source and drain electrodes confront each other;

a passivation layer covering the thin film transistor wherein a contact hole exposing a portion of the drain electrode is formed in the passivation layer; and

a pixel electrode formed on the passivation layer and being connected to the drain electrode through the contact hole, wherein the pixel electrode partially overlaps the data line;

a color filter plate including a black matrix, a color filter and a common electrode on a second transparent substrate; and

liquid crystals [[injected]] provided and sealed between the thin film transistor plate and the color filter plate,

wherein a cut-off film is formed under the data line, said cut-off film being asymmetrically overlapped by the data line and being partially overlapped by the pixel electrode according to an alignment direction.

11. (Original) The liquid crystal display according to claim 10, wherein the passivation layer is an organic passivation layer.

12. (Original) The liquid crystal display according to claim 10, wherein the cut-off film and the gate line are formed on a same level.

13. (Currently Amended) The liquid crystal display according to claim 10, wherein an overlap region between the pixel electrode, the cut-off layer and the data line [[range]] has a width [[of]] between 2μm and 4μm.

14. (Original) The liquid crystal display according to claim 10, wherein the cut-off film is formed at one side of the data line, said side selected according to a direction of rubbing an alignment film.

15. (Currently Amended) A method of fabricating a liquid crystal display having a transparent substrate on which a gate line region and a data line region are defined, comprising:

simultaneously forming a gate line in the gate region wherein a gate electrode protrudes from the gate line, and a cut-off film which is asymmetrically overlapped by the data line region according to an alignment direction of an alignment film;

forming a data line in the data line region on the transparent substrate, wherein the data line crosses and is insulated from the gate line, and wherein a source electrode is formed at one side of the data line, and wherein a drain electrode is formed which confronts and is isolated from the source electrode;

forming a passivation layer covering the gate line region, the data line region and the cut-off film, wherein a contact hole exposing a portion of the drain electrode is formed in the passivation layer; and

forming a pixel electrode connected to the drain electrode through the contact hole on the passivation layer, the pixel electrode being asymmetrically overlapped with the data line region according to the alignment direction of the alignment film, wherein the pixel electrode partially overlaps the cut-off film.

16. (Original) The method according to claim 15, wherein the passivation layer is an organic passivation layer.

17. (Original) The method according to claim 15, wherein the cut-off film and the gate line are formed on a same level.

18. (Original) The method according to claim 15, an overlap region between the pixel electrode, the cut-off layer and the data line range has a width of between 2μm and 4μm..

19. (Currently Amended) The method according to claim 6, wherein a first overlap width between the first data line and the pixel electrode is larger than a second overlap width between the pixel electrode and the second date line [[15, wherein the cut-off film is formed at one side of the data line, said side selected according to a direction of rubbing an alignment film]].

20. (New) A liquid crystal display comprising:

a first transparent substrate;

a gate line on the first transparent substrate;

a data line arranged to cross the gate line wherein the gate line is insulated from the date line;

a thin film transistor having a source electrode connected to the data line, a drain electrode separated from the source electrode, and a gate electrode connected to said gate line in an area where said data line crosses said gate line;

a passivation layer over the thin film transistor and having a contact hole exposing a portion of the drain electrode; and

a pixel electrode formed on the passivation layer and being connected to the drain electrode through the contact hole, the pixel electrode asymmetrically overlapping with the data line according to an alignment direction of an alignment layer;

a cut-off film under the data line, the cut-off film being asymmetrical with the data line according to the alignment direction of the alignment layer;

a second transparent substrate including a black matrix, a color filter and a common electrode; and

liquid crystals between the first and second transparent substrates.